REMARKS

Claims 1 through 22 are currently pending in the application.

This amendment is in response to the Office Action of December 4, 2002.

Preliminary Amendment

Applicants' undersigned attorney notes the filing herein of a Preliminary Amendment on January 22, 2002, which filing was not acknowledged in the outstanding Office Action. Should the Preliminary Amendment have failed for some reason to have been entered in the Office file, Applicants' undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner.

35 U.S.C. § 101 Double Patenting Rejection

Claims 1 through 22 stand rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 7 through 28 of prior U.S. Patent 6,084,288 (hereinafter referred to as the `288 patent). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants submit that a reliable test for statutory double patenting under 35 U.S.C. § 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting under 35 U.S.C. § 101 does not exist. *In re Vogel*, 422 F.2d 438, 164 USPQ 619(CCPA 1970).

In the present instance, amended independent claims 1 and 6 of the present application are directed to embodiments of the inventions that are different than the embodiments of the inventions set forth in corresponding claims 1 and 6 of the `288 patent. For instance, presently amended independent claim 1 of the present application is directed to an embodiment of the invention having an element of the invention calling for "removing a portion of the third coating" whereas the embodiment of the invention set forth in claim 7 of the `288 patent contains has no such element of the invention. Similarly, presently amended independent claim 6 of the present application is directed to an embodiment of the invention having an element of the invention

calling for "etching a portion of the wafer substrate" whereas claim 12 of the `288 patent contains no such element of the invention. Accordingly, no statutory double patenting exists or can exist between claims 1 through 22 of the present application and claims 2 through 28 of the `288 patent. Therefore, claims 1 through 22 are allowable.

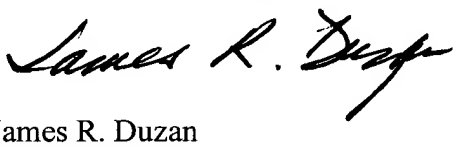
Double Patenting Rejection

Claims 1 through 22 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 22 of U.S. Patent 6,287,942 B1. In order to avoid further expenses and time delay, Applicants elect to expedite the prosecution of the present application by filing a Terminal Disclaimer to obviate the double patenting rejections in compliance with 37 CFR §1.321 (b) and (c). Applicants' filing of the Terminal Disclaimer should not be construed as acquiescence of the Examiner's double patenting or obviousness-type double patenting rejections. Attached are the Terminal Disclaimer and accompanying fee.

In summary, Applicants submit that claims 1 through 22 are clearly allowable.

Applicants request the allowance of claims 1 through 22 and the case passed for issue.

Respectfully submitted,



James R. Duzan
Registration No. 28,393
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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JRD/jml:djp

Enclosure: Version with Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A sealing method for at least one semiconductor device on a first side of a wafer substrate, the wafer substrate having the first side, a second side, and a thickness, the at least one semiconductor device having a plurality of sides and at least one bond pad thereon, said sealing method comprising:

reducing the thickness of at least a portion of the wafer substrate from the second side thereof;

coating the first side of the wafer substrate using a first coating to substantially seal the at least one semiconductor device on the first side of the wafer substrate;

removing a portion of the wafer substrate from each of the plurality of sides of the at least one semiconductor device on the first side of the wafer substrate, the portion of the wafer substrate being removed extending from the second side of the wafer substrate to the coating on the first side of the wafer substrate;

coating the second side of the wafer substrate using a second coating to substantially seal the second side of the wafer substrate and to substantially seal the plurality of sides of the at least one semiconductor device;

removing a portion of the first coating on the first side of the wafer substrate for uncovering a portion of the at least one bond pad located on the at least one semiconductor device; [and]

applying a third coating to the at least one bond pad of the at least one semiconductor device, the third coating substantially sealingly engaging the at least one bond pad and substantially sealing the first coating; and

removing a portion of the third coating.

6. (Twice Amended) A sealing method for at least one semiconductor device on a first side of a wafer substrate, the wafer substrate having the first side, a second side, and a thickness, the at least one semiconductor device having a plurality of sides and at least one bond pad thereon, said sealing method comprising:

coating the first side of the wafer substrate with a first coating to substantially seal the at least one semiconductor device on the first side of the wafer substrate;

reducing the thickness of at least a portion of the wafer substrate from the second side thereof by thinning the wafer substrate in at least the portion of the wafer substrate located on said at least one semiconductor device;

removing a portion of the wafer substrate from each of the plurality of sides of the at least one semiconductor device on the wafer substrate by removing a portion of the wafer substrate extending through the thickness thereof; [and]

coating the second side of the wafer substrate with a second coating; and

etching a portion of the wafer substrate.